REMARKS

Claims 1, 3-27 and 29-34 are currently pending in the subject application and are presently under consideration. Claims 1, 23, 33 and 34 have been amended. Claims 10 and 32 have been canceled. A version of these claims is on pages 2-7 of this Reply.

Accordingly, no new matter has been introduced, no new search is required, and it is respectfully submitted that the amendments should be entered. Favorable reconsideration of the subject patent application is respectfully requested in view of the amendments and comments herein.

I. Rejection of Claims 1, 3-27 and 29-34 Under 35 U.S.C. §102(e)

Claims 1, 3-27 and 29-34 stand rejected under 35 U.S.C. §102(e) as being anticipated by Mieher *et al.* (U.S. App. 2004/0257571). Withdrawal of this rejection is requested for at least the following reasons. Mieher *et al.* does not anticipate each and every element as set forth in the subject claims.

> A single prior art reference anticipates a patent claim only if it expressly or inherently describes each and every limitation set forth in the patent claim. *Trintec Industries, Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the ... claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants' invention generally relates to a multi-layer overlay measurement and correction technique for integrated circuit manufacturing. Independent claims 1, 23, 33, and 34 recite similar limitations, namely, a method and system for facilitating measurement and correction of overlay between multiple layers of a wafer, comprising: an overlay target, a measurement component that generates images/signatures of an overlay target, a comparison component that compares the images/signatures of the overlay target with one or more stored images/signatures, and *a control component or correction of overlay error step that utilizes the overlay error determined by the measurement component to correct overlay error between the three or more layers of the wafer, **the control component facilitates concurrent overlay***

correction of two or more wafers. Mieher *et al.* does not expressly or inherently disclose the aforementioned novel aspects of applicants' invention as recited in the subject claims.

Mieher *et al.* generally relates to apparatus and methods for detecting overlay errors using scatterometry. Mechanisms are provided for determining overlay error between two layers of a sample using improved scatterometry overlay techniques. This scatterometry overlay data may then be used to generate correctables for the particular lithography tool. (*See* pg. 23, paragraph [0259]). The overlay results obtained with scatterometry overlay techniques may also be used to calculate corrections to the stepper setting to minimize overlay error. The overlay errors are input to an automated process control system which may then calculate a set of stepper corrections to input to the stepper to minimize the overlay errors for subsequent wafer processing. (*See* pg. 28, paragraph [0306]).

The Examiner contends that Mieher *et al.* anticipates claims 1, 3-27 and 29-34. Specifically, the Examiner contends that Mieher *et al.* discloses a control component (or corrective step) that facilitates concurrent overlay correction of two or more wafers. The applicants' representative respectfully disagrees for at least the following reasons. Mieher *et al.* discloses apparatus and methods for detecting overlay errors using scatterometry, but Mieher *et al.* is silent with respect to ***a control component or correction of overlay error step that facilitates concurrent overlay correction of two or more wafers***, a limitation included in independent claims 1, 23, 33, and 34 of the subject invention.

Mieher *et al.* limits itself to ***apparatus and methods for detecting overlay errors*** using scatterometry to minimize the overlay errors for subsequent wafer processing. *See* para. [0306]. Mieher et al. does not disclose the concurrent overlay correction of two or more wafers. For example, the measurements obtained by the measurement component of the present invention can be concurrently utilized as both feed-back and feed-forward information, thus enabling correction of overlay of multiple wafers concurrently. Whereas, the paragraphs cited by the Examiner to support this limitation do not disclose the concurrent overlay correction of multiple wafers. Paragraph [0110] discloses the implementation of the scatterometry system in an overlay metrology system as an additional overlay measurement capability. Thus, allowing the combination of overlay data from imaging overlay measurements and scatterometry overlay measurements. Paragraph [0259] discloses that the scatterometry and imaging overlay data may also be used to generate correctables for the particular lithography tool. The data can be

translated into parameters, for correcting the lithography tool. Paragraph [0306] discloses utilizing the scatterometry overlay data to minimize the overlay errors for subsequent wafer processing. As such, nowhere does Mieher *et al.* disclose the ***concurrent overlay correction of two or more wafers***.

In view of at least the above, it is readily apparent that Mieher *et al.* fails to expressly or inherently disclose applicants' claimed invention as recited in independent claims 1, 23, 33 and 34 (and claims 3-9, 11-22 and 24-31 which respectively depend there from). Accordingly, it is respectfully requested that these claims be deemed allowable.

CONCLUSION

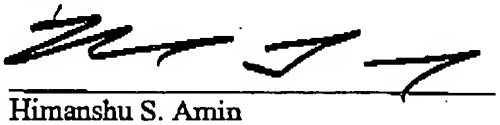
The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP986US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

AMIN & TUROCY, LLP



Himanshu S. Amin
Reg. No. 40,894

AMIN & TUROCY, LLP
24TH Floor, National City Center
1900 E. 9TH Street
Cleveland, Ohio 44114
Telephone (216) 696-8730
Facsimile (216) 696-8731